

**IN THE CLAIMS**

Please amend the claims as shown below:

1-11. (Cancelled)

12. (Currently amended) An integrated circuit, fabricated using the method comprising:

creating a customized description language model of an integrated circuit design by:

~~editing a first file specific to said design;~~

~~defining the location of at least one library file;~~

~~generating a script using said first file, said library file, and user input information; and~~

~~running said script to create said customized description language model;~~

receiving one or more inputs from a user for at least one customized parameter of the integrated circuit;

receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated; and

generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter;

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

fabricating at least one mask or FPGA configuration file representing said compiled integrated circuit design;

and

fabricating said integrated circuit using said at least one mask or FPGA configuration file;

wherein said act of creating is performed at a high level of abstraction.

13. (Currently amended) The integrated circuit of claim 12, wherein the act of receiving one or more inputs editing comprises receiving input of one or more parameters by a user selecting at least one of a plurality of input parameters associated with said design, said at least one parameter being selected from the group comprising:

- (i) custom instruction sets;
- (ii) cache configurations;
- (iii) memory interface configurations; and
- (iv) system architecture configurations.

14. (Previously presented) The integrated circuit of claim 12, wherein the act of generating a netlist comprises generating a list of logic devices and their interconnections.

15. (Previously presented) The integrated circuit of claim 12, wherein the act of fabricating said integrated circuit comprises defining physical features on a semi- conductive substrate via a lithographic process.

16. (Previously presented) The integrated circuit of claim 12, further comprising synthesizing said design based on said description language model.

17. (Currently amended) The integrated circuit of claim 13, wherein the act of receiving inputs editing is performed interactively with the user using a display.

18. (Currently amended) An apparatus adapted to generate integrated circuit designs, comprising:

a processor capable of running a computer program;

a storage device operatively coupled to said processor, said storage device being capable of storing at least a portion of a computer program;

an input device, operatively coupled to said processor capable of receiving input from a user and transmitting said input to said processor; and

a computer program resident at least in part on said storage device, said computer program adapted to ~~receive said input relating to a constrained set of design variables relating to a basecase processor configuration from said user and~~ perform the following acts based on said input:

~~editing a first file specific to said integrated circuit design;~~

~~defining the location of at least one library file;~~

~~generating a script using said first file, said library file, and user input information; and~~

~~running said script to create said description language model of said integrated circuit design~~

receiving one or more inputs from a user for at least one customized parameter of the integrated circuit;

receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated; and

generating a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

19. (Previously presented) The apparatus of claim 18, wherein said description language model is a hardware description language (HDL).

20. (Currently amended) The apparatus of claim 18, wherein said computer program is further adapted to perform the acts comprising:

generating a ~~second~~ file based on said description language model for use with a simulation; and

simulating said design using said ~~second~~ file.

21. (Previously presented) The apparatus of claim 20, wherein said computer program is further adapted to perform the act comprising running synthesis scripts based on said description language model in order to synthesize said integrated circuit design.

22. (Previously presented) The apparatus of claim 18, wherein said processor comprises a digital microprocessor, and said storage device comprises magnetic media.

23.-39. (Canceled)

40. (Currently amended) A system for generating integrated circuit designs at a high level of abstraction comprising:

a processor;

a storage device in data communication with said processor, said storage device being capable of storing and retrieving a computer program; and

a computer program stored within said storage device and adapted to run on said processor, said computer program comprising;

~~a user configurable macro instruction having at least a first user selectable element, said first selectable element being selected from the group comprising:~~

- ~~(i) a plurality of custom instructions;~~
- ~~(ii) a plurality of cache configurations;~~
- ~~(iii) a plurality of memory interface configurations; and~~
- ~~(iv) a plurality of system architecture configurations;~~

~~a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element; and~~

~~a second algorithm capable of running said script to generate a description language model of an integrated circuit design~~

an input receiving module that receives one or more inputs from a user for at least one customized parameter of an integrated circuit device, the at least one customized parameter comprising a parameter selected from the group comprising a custom instruction, a cache configuration, a memory interface configuration and a system architecture configuration;

a library file receiving module that receives an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated; and

a generation module that generates a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description through acts including reading at least one prototype description and modifying the at least one prototype description by substituting values in the at

least one prototype description or merging additional descriptions based on the at least one customized parameter.

41. (Currently amended) The system of claim 40, wherein said computer program further comprises a ~~second~~-user-selectable element, said ~~second~~-user-selectable element allowing said user to select one of a plurality of process technology options.

42. (Previously presented) The system of claim 40, wherein ~~said first user selectable element is selected~~ the input receiving module receives input by the act of reading a pre-configured data file.

43.-46. (Canceled)

47. (Currently amended) A method of generating the design of an integrated circuit rendered in a hardware description language, said method being performed at a high level of abstraction and comprising the acts of:

selecting a process technology;

receiving one or more inputs from a user for at least one customized parameter of the integrated circuit, including at least one ~~editing a first file specific to the design, said act of editing comprising selecting at least one user configurable parameter~~ selected from the group comprising:

- (i) processor instructions;
- (ii) cache configuration;
- (iii) memory interface configuration; and
- (iv) system architecture configuration;

receiving an identification of a ~~defining the~~ location of at least one library file that provides at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated; and

~~generating a script using said first file and said library;~~

~~running said script to create a customized hardware description language model of the design; and~~

~~running a synthesis algorithm to synthesize a file descriptive of said design~~

generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

48. (Currently amended) A system for generating integrated circuit designs at a high level of abstraction, comprising:

means for processing digital data;

means for data storage in data communication with said processor means, said means for data storage being capable of storing and retrieving a computer program; and

a computer program stored within said means for data storage and adapted to run on said processor means, said computer program comprising:

means for selecting a process technology;

an input receiving module that receives one or more inputs from a user for at least one customized parameter of the integrated circuit device, including at least one parameter -a

~~user configurable macro instruction having at least one user selectable element, said user-selectable element being selected from the group comprising a cache configuration, a memory interface configuration, and a system architecture configuration;~~

~~(i) a plurality of instructions;~~

~~(ii) a plurality of cache configurations;~~

~~(iii) a plurality of memory interface configurations; and~~

~~(iv) a plurality of system architecture configurations;~~

~~means for generating a script based on said user selectable element and said process technology; and~~

~~means for running said script to generate a description language model of an integrated circuit design~~

a library file receiving module that receives an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated; and

a generation module that generates a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description through acts including reading one or more prototype description and modifying the one or more prototype description by substituting values in the one or more prototype description or merging additional descriptions based on the at least one customized parameter.

49-59. (Canceled)

60. (Currently amended) A method of designing a configurable processor, the method comprising:



receiving an identification of one or more pre-defined instructions described in a hardware description language for the configurable processor and at least one user-defined extension description, described in user-supplied hardware description language;

generating, at a high level of abstraction, a processor specification based on one or more of the pre-defined instructions described in a hardware description language and including having a user-definable portion based on the at least one user-defined extension description, the user-definable portion of said specification including at least one user-defined instruction having a function associated therewith; and

based on said processor specification, generating a description of a hardware implementation of said configurable processor.

61. (Previously presented) The method of claim 60, wherein said act of generating a description comprises generating a description including control logic necessary for the execution of said at least one user-defined instruction.

62. (Previously presented) The method of claim 61, wherein said act of generating a description of a hardware implementation comprises describing at least an instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages.

63. (Previously presented) The method of claim 60, wherein said act of generating a description comprises generating a description having at least one element selected from the group consisting of:

(i) registers; (ii) condition code choices; and (iii) scratchpad RAM.

64. (Previously presented) The method of claim 60, wherein said act of generating a description comprises generating a description having at least one library of multimedia extensions.

65. (Previously presented) The method of claim 60, further comprising simulating said configurable processor using at least said description.

66. (Previously presented) The method of claim 65, wherein said act of simulating comprises:

- running at least one script to generate simulation data;
- running at least one simulation using at least said simulation data; and
- determining the adequacy of said configurable processor based at least in part on said act of running.

67. (Previously presented) The method of claim 60, further comprising synthesizing said configurable processor using at least said description.

68. (Previously presented) The method of claim 67, wherein said act of synthesizing comprises:

- running at least one synthesis script to generate synthesis data;
- and evaluating the adequacy of said synthesis data based at least in part on at least one design criterion.

69. (Previously presented) The method of claim 68, wherein said at least one design criterion comprises:

- at least one specific processor performance criterion; and
- at least one processor die size criterion.

70. (Previously presented) The method of claim 68, further comprising:

revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate;

re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data;

and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion.

71. (Previously presented) The method of claim 70, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising comprises revising at least one library.

72. (Previously presented) The method of claim 71, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising further comprises revising at least one control file.

73. (Previously presented) The method of claim 70, wherein said at least one design criterion comprises processor clock speed, and said act of revising comprises revising at least one library.

74. (Previously presented) The method of claim 70, wherein said at least one design criterion comprises processor power consumption, and said act of revising comprises revising at least one netlist (net load).

75. (Currently amended) A computer-implemented method of generating the design of an integrated circuit at a high level of abstraction using a description language, comprising the acts of:

providing an existing processor core configuration;

receiving one or more inputs from a user for at least one customized parameter of the existing processor core configuration for the integrated circuit device, the input being selected from a ~~editing a first file specific to the design, said editing comprising selecting a constrained~~ set of input parameters associated with said configuration, said parameters comprising:

- (i) at least one custom instruction;
- (ii) a cache configuration; and
- (iii) a memory interface configuration;

~~providing at least one library file;~~

~~generating a script using said first file, said library file, and user input information;~~

~~running said script to create a customized description language model; and~~

~~synthesizing said design based on said description language model~~

receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated; and

generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

76. (Currently amended) A method of generating an integrated circuit design at a high level of abstraction, comprising:

providing a user with a plurality of optional inputs instructions, including the ability to generate a customized hardware description language code instruction;

selecting at least one of said plurality of optional inputs instructions;

selecting at least one cache configuration;

defining at least one memory interface;

~~generating a script based on said at least one optional instruction, cache configuration, and memory interface; and~~

~~running said script to generate a hardware description language model of said integrated circuit design~~

generating through an automated process a customized description language model based on at least one optional input, cache configuration, and memory interface customized parameter, the automated process including the acts of reading at least one prototype description, modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one optional input, cache configuration and memory interface, and incorporating any customized hardware description language code instructions.

77. (Currently amended) A description language model of an integrated circuit design generated at a high level of abstraction using the method comprising:

receiving one or more inputs from a user for at least one customized parameter of the existing processor core configuration for the integrated circuit device, the input being selected from a ~~editing a first file specific to said integrated circuit design including selecting a plurality~~ of input parameters associated with said design, said parameters comprising:

(i) at least one extension instruction; and

(ii) a cache configuration;

defining the location of at least one library file that provides at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated; and;

~~generating a script using said first tile, said library tile, and user input information; and  
running said script to create said description language model of said integrated circuit design;~~

~~wherein said method is performed at a high level of abstraction~~

generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

78. (Currently amended) A method of generating an extended processor design at a high level of abstraction, comprising:

providing the user with a basecase processor core configuration having a base instruction set;

providing a user with a plurality of optional instructions adaptable for use with said basecase core;

receiving the selection of ~~selecting~~ at least one of said plurality of optional instructions;

receiving the selection of ~~selecting~~ at least one cache configuration;

~~generating a script based on said at least one optional instruction, cache configuration,~~  
~~and basecase core; and~~

~~running said script to generate a hardware description language model of said processor~~  
~~design;~~

receiving an identification of a location of one or more library files that provide at least  
one basecase description and at least one extension logic description for the integrated circuit  
device for which a model is being generated;

generating through an automated process a customized description language model based  
on at least one optional instruction, the at least one basecase description, and the at least one  
extension logic description, the automated process including the acts of reading at least one  
basecase description and modifying the at least one basecase description by substituting values in  
the at least one basecase description or merging additional descriptions based on the at least one  
customized parameter; and

wherein said plurality of optional instructions and cache configurations are constrained so  
as to ensure the functionality of said processor design irrespective of the user's selections.

79. (Newly added) A computer-implemented method of generating a  
customized description language model of a integrated circuit design including at least one of a  
microprocessor or microprocessor peripheral device comprising the following acts performed by  
a computer process:

receiving one or more inputs from a user for at least one customized parameter of the  
microprocessor or microprocessor peripheral;

receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the microprocessor or microprocessor peripheral for which a model is being generated; and

generating through an automated process a customized description language model based on the least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one of the prototype descriptions and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

80. (Newly added) The method of claim 79 where the inputs are received through an interactive process.

81. (Newly added) The method of claim 79 wherein the inputs are received in a non-description language format.

82. (Newly added) The method of claim 79 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

83. (Newly added) The method of claim 79 wherein the generating act comprises copying one or more prototype files, substituting chosen and calculated values in those prototype files and merging in additional hardware language description language to the prototype file.

84. (Newly added) The method of claim 79 wherein the description language is written in steps.



85. (Newly added) A method of designing an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising the acts of:

receiving one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the microprocessor or microprocessor peripheral for which a model is being generated;

generating through an automated process a customized description language model based on the least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter;

testing the customized description language through simulation or synthesis; and

if a different testing outcome is desired, receiving an identification of one or more input for at least one customized parameter and generating a second customized description language model.

86. (Newly added) The method of claim 85 where the inputs are received through an interactive process.

87. (Newly added) The method of claim 85 wherein the inputs are received in a non-description language format.

88. (Newly added) The method of claim 85 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

89. (Newly added) The method of claim 85 wherein the generating act comprises copying one or more prototype files, substituting chosen and calculated values in those prototype files and merging in additional hardware language description language to the prototype file.

90. (Newly added) The method of claim 85 wherein the description language is written in steps.

91. (Newly added) An apparatus that generates a customized description language model of an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising:

an input module that receives one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

a library file module that receives an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated; and

a description language model generator that generates a customized description language model based on the least one customized parameter, the at least one prototype description and the at least one extension logic description through an automated process that reads at least one prototype description and modifies the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter.

92. (Newly added) The apparatus of claim 91 where the inputs are received through an interactive process.
93. (Newly added) The apparatus of claim 91 wherein the inputs are received in a non-description language format.
94. (Newly added) The apparatus of claim 91 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.
95. (Newly added) The apparatus of claim 91 wherein the generator copies one or more prototype files, substitutes chosen and calculated values in those prototype files and merges in additional hardware language description language to the prototype file.
96. (Newly added) The apparatus of claim 91 wherein the description language is written in steps.
97. (Newly added) An apparatus that generates a customized description language model of an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising:
- an input module that receives one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;
  - a library file module that receives an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated;
  - a description language model generator that generates a customized description language model based on the least one customized parameter, the at least one prototype description and the at least one extension logic description through an automated process that reads at least one

prototype description and modifies the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter; and

a feedback module that enables a user to test the customized description language through simulation or synthesis; and

wherein if a different testing outcome is desired, the input receiving module enables the user to input an identification of one or more input for at least one customized parameter and the description language generator generates a second customized description language model.

98. (Newly added) The method of claim 97 where the inputs are received through an interactive process.

99. (Newly added) The method of claim 97 wherein the inputs are received in a non-description language format.

100. (Newly added) The method of claim 97 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

101. (Newly added) The method of claim 97 wherein the generator copies one or more prototype files, substitutes chosen and calculated values in those prototype files and merges in additional hardware language description language to the prototype file.

102. (Newly added) A computer-implemented method of generating a customized description language model and associated test code of a integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising the following acts performed by a computer process:

receiving one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

generating through an automated process a customized description language model based on the least one customized parameter, the automated process including the act of modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter;

generating through an automated process test code associated with the customized description language model based on the at least one customized parameter.

103. (Newly added)        The method of claim 102 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

104. (Newly added)        A method of designing an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising the acts of:

receiving one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

generating through an automated process a customized description language model based on the least one customized parameter, the automated process including the act of modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter;

generating through an automated process test code associated with the customized description language model based on the at least one customized parameter

testing the customized description language through simulation or synthesis using the test code generated; and

if a different testing outcome is desired, receiving an identification of one or more input for at least one customized parameter and generating a second customized description language model.

105. (Newly added) The method of claim 104 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

106. (Newly added) An apparatus that generates a customized description language model of an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising:

an input module that receives one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

a description language model generator that generates through an automated process a customized description language model based on the least one customized parameter, the automated process including the act of modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter; and

a test code generator that generates through an automated process test code associated with the customized description language model based on the at least one customized parameter.

107. (Newly added) The apparatus of claim 106 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

108. (Newly added)      An apparatus that generates a customized description language model of an integrated circuit design including at least one of a microprocessor or microprocessor peripheral device comprising:

an input module that receives one or more inputs from a user for at least one customized parameter of the microprocessor or microprocessor peripheral;

a description language model generator that generates through an automated process a customized description language model based on the least one customized parameter, the automated process including the act of modifying at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter;

a test code generator that generates through an automated process test code associated with the customized description language model based on the at least one customized parameter;

a feedback module that enables a user to test the customized description language through simulation or synthesis using the test code generated; and

wherein if a different testing outcome is desired, the input receiving module enables the user to input an identification of one or more input for at least one customized parameter and the description language generator generates a second customized description language model.

109. (Newly added)      The method of claim 108 wherein the customized description language model includes both functional and structural description language descriptions for the microprocessor or microprocessor peripheral.

110. (Newly added)      The method of claim 79, wherein said one or more inputs received from the user are received via a graphical user interface (GUI).

111. (Newly added) The method of claim 79, wherein the method further comprises conducting a hardware/software co-verification.

112. (Newly added) The method of claim 79, wherein the act of conducting a hardware/software co-verification further comprises using a debugger to run software using at least a portion of the description language model.

113. (Newly added) The method of claim 79, wherein the method further comprises conducting a core verification as part of the act of generating a customized description language model.

114. (Newly added) The apparatus of claim 91, wherein said one or more inputs received from said user are received via a graphical user interface (GUI).

115. (Newly added) The apparatus of claim 91, wherein the method further comprises conducting a hardware/software co-verification.

116. (Newly added) The apparatus of claim 91, wherein the act of conducting a hardware/software co-verification further comprises using a debugger to run software using at least a portion of said description language model.

117. (Newly added) The apparatus of claim 91, wherein the method further comprises conducting a core verification as part of the act of generating a customized description language model.